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NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE. WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98  
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.  
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .004"/.0044"

7. PLATING FINISH: A. INMERSION GOLD: 2-8 MICROINCHES OF GOLD OVER 100-250 MICROINCHES MINIMUM NICKEL.

8. FAB VENDOR IS NOT ALLOWED TO USE ODB FOR FABRICATION. CAN BE USED ONLY FOR REFERENCE.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).  
GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.  
TYPE: LPI OR EQUIVALENT.  
A. LOCATION ± +/--.002" OF PLATED PADS.  
B. DIAMETER OR SIZE ± +/--.002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS.  
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.  
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (Pb)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/--.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS. KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

22. THIS BOARD USES VIA-IN-PAD: SEE FAB\_VIAFILL.ART  
A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.  
B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.  
C. DIMPLE ON VIA-IN-PADS MUST BE NO GREATER THAN .003" AND PROTRUSION NO GREATER THAN .002"

23. INTENTIONAL 29 SHORTS AT:

LocationStart	LocationEnd	RefDes	Net 1	Net 2
(210.00 303.00)	(210.00 343.00)	SH1	RESET	RST_TGTCMU_B
(110.00 303.00)	(110.00 343.00)	SH2	AN	ADC_IN
(131.26 936.26)	(131.26 1015.00)	JS5	UART0_RX	UART_RX
(210.00 1015.00)	(210.00 936.26)	JS6	UART0_TX	UART_TX
(66.00 980.00)	(66.00 1020.00)	SH3	PTD2/TMP1_CHO	PWM
(97.24 1301.26)	(97.24 1380.00)	JS4	P5V_CAN	FL_USB_SVO
(310.00 303.00)	(310.00 343.00)	SH4	SPI_PSC0	LPSP1_PCS0
(410.00 303.00)	(410.00 343.00)	SH6	SPI_SCK	LPSP1_SCK
(470.00 1060.00)	(510.00 1060.00)	SH11	I2C1_SCL	I2C_SCL
(295.00 1060.00)	(335.00 1060.00)	SH5	WU00_P12/NMI_B	LLWU/NMI_B
(682.80 31.26)	(682.80 110.00)	JS2	P_LED	V_BRD
(610.00 303.00)	(610.00 343.00)	SH10	SPI_SOUT	LPSP1_SOUT
(510.00 303.00)	(510.00 343.00)	SH8	SPI_SIN	LPSP1_SIN
(570.00 1060.00)	(610.00 1060.00)	SH13	PTD3/I2C1_SDA	I2C_SDA
(710.00 300.00)	(710.00 340.00)	SH12	3V3_MIKROE	V_BRD
(750.00 1060.00)	(710.00 1060.00)	SH14	P5V	5V_MIKROE
(1095.71 -2.04)	(1095.71 -80.78)	JS14	TMP1_CHO	LED1_B1
(1498.86 1619.02)	(1498.86 1682.02)	SH19	P3V3_LDO	V_BRD
(1802.41 505.60)	(1762.41 505.60)	SH15	V_BRD	VCC_TGMCU
(1782.74 1781.74)	(1782.74 1741.74)	SH21	VDD_IC	P_VDD_SWITCH
(1849.10 -7.06)	(1849.10 55.94)	SH20	BOOT_CFG	SWO/BOOT_CFG
(2094.30 1414.97)	(1994.30 1414.97)	JS11	UART1_TX	N23938761
(2094.30 1289.97)	(1994.30 1289.97)	JS10	UART1_RX	N23938720
(2094.30 1539.97)	(2015.56 1539.97)	JS1	VDD_MEM	V_BRD
(2454.01 318.43)	(2454.01 358.43)	SH22	N24374306	VDD_DCDC
(2445.41 1289.97)	(2485.41 1289.97)	SH23	N24374396	VDD_RF
(2620.82 80.95)	(2620.82 159.69)	JS3	RST_TGTCMU_B	LED_RTS
(2672.48 922.47)	(2732.48 922.47)	SH24	RF_GPO_5	N24516334
(2722.41 424.47)	(2722.41 484.47)	SH9	RF_GPO_4	N24441947

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DESIGN CROSS SECTION CHART

TOTAL THICKNESS 58.9 MIL

BOARD THICKNESS TOLERANCE +/-10%  
ALL VALUES ARE FINISHED VALUES

DETAIL A  
LAYER STACKUP  
SCALE: NONE

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DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
+	8.0	+0.0/-8.0	PLATED	1488
⊖	8.1	+0.0/-8.1	PLATED	193
○	16.0	+2.0/-2.0	PLATED	16
⊗	28.0	+2.0/-2.0	PLATED	20
⬢	35.0	+2.0/-2.0	PLATED	5
⬢	35.0	+3.0/-3.0	PLATED	57
⊗	40.0	+2.0/-2.0	PLATED	8
⬢	40.0	+3.0/-3.0	PLATED	30
⬢	63.0	+3.0/-3.0	PLATED	1
⊗	100.0	+2.0/-2.0	NON-PLATED	1
⊗	118.0	+2.0/-2.0	NON-PLATED	2
⬢	55.0x24.0	+2.0/-2.0	PLATED	2
⬢	83.0x24.0	+2.0/-2.0	PLATED	2
⬢	111.0x32.0	+2.0/-2.0	PLATED	3
⬢	122.0x32.0	+2.0/-2.0	PLATED	2

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PART NO.  
170-93460

NXP SEMICONDUCTORS

6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

COMPANY PUBLIC

COMPANY INTERNAL

COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED  
DIMENSIONS ARE IN INCHES  
TOLERANCES ARE:  
DECIMALS ANGLES  
.XX .01 .030  
.XXX .005

ALL PARTS, MATERIALS AND FINISHED  
ASSEMBLY SHALL MEET THE R&D  
COMMISSION DELEGATED DIRECTIVE (EU)  
2015/494 OF 31 MARCH 2015 AMENDING  
ANNEX I TO DIRECTIVE 2011/65/EU. A  
REQUIREMENT FOR COMPLIANCE IS  
REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED  
ASSEMBLY SHALL NOT CONTAIN ANY OF  
THE SUBSTANCES OF VERY HIGH CONCERN  
LISTED ABOVE THE THRESHOLD VALUE PER  
THE CURRENT ECHA LIST OF SVHC'S AND  
WITH AN X-10 AND ANNE 1011 OF EACH  
SUBSTANCE IS REQUIRED UPON REQUEST.

APPROVALS

DATE

TITLE

DRAWN  
MARIA ECHEVARRIA

09-18-25

CHECKED  
JORGE RODRIGUEZ

09-18-25

DESIGN ENGINEER  
ANTONIO QUIROZ

09-18-25

SIZE

CAD FILE NAME

DWG. NO.

REV

D

LAY-93460

FAB-93460

D

SCALE

DO NOT SCALE DRAWING

SHEET 1 OF 2

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